Amendments to the Specification:

Please replace paragraphs **[0005]**, **[0023]** and **[0033]** with the following:

[0005] In many semiconductor applications, formation of conductive bumps or other external conductive elements on the bond pads of a die is desirable, if not necessary, to connect the die to external conductors. The most common applications where conductive bumps or other elements are used include tape automated bonding (TAB), flip-chip attachment of a die to a carrier substrate, and direct chip attachment (DCA) of a die to a carrier substrate. Conductive bumps may comprise metals or alloys including, without limitation, conventional ~~tin\lead~~ tin/lead solders, or may comprise conductive or conductor-filled epoxies, all as known in the art. Formation of the conductive bumps used in these applications can be accomplished using a variety of commonly known methods, such as deposition onto bond pads by screening or printing, preform ball or bump placement, or ball bumping using wire bonding equipment to form each individual bump *in situ*.

[0023] Semiconductor substrate 10 may comprise a wafer, as defined above, including a plurality of individual die locations thereon. The bond pads 12 are "bumped" with intermediate conductive elements 20 which project upwardly from active surface 14, or some or all of the input\output locations for each die are redistributed using conductive traces prior to being bumped, such processes being well known in the art. If the external conductive elements (see below) are metallurgically incompatible with bond pads 12, the intermediate conductive elements 20 may be of a layer or layers of metals which will provide a better metallurgical bond therebetween. One such example, in the case of Al bond pads and ~~tin\lead~~ tin/lead solder external conductive elements, would be to form intermediate conductive elements 20 of three superimposed layers (top to bottom) of copper, copper/chromium alloy, and chromium. It is also contemplated that the bond pads 12 may be bumped using a wire bonding capillary, or with solder of a higher melting temperature than that of another solder to be employed in external conductive elements 32, as referenced below. Intermediate conductive elements 20 may also comprise a conductive or conductor-filled epoxy, such as a silver-filled epoxy. The only

significant constraints on the material and configuration selected for intermediate conductive elements 20 are compatibility with the bond pads 12 or other input\output contacts on substrate 10 as well as with external conductive elements 32, and sufficient temperature tolerance and physical strength to withstand encapsulation of active surface 14 of substrate 10 and formation of external conductive elements 32 thereon.

[0033] FIG. 2 depicts how encapsulant material 30 may be applied to both the active surface 14 and the back side 22 of semiconductor substrate 10 in a substantially conformal manner so as to fill in channels or troughs 26, but not to overfill same to the point of being level with the top surfaces of intermediate conductive elements 20. The depressions 29 (shown in FIGS. 1C-1E by broken lines) of the encapsulant material 30 over channels or troughs 26 are useful in that during the dicing operation, the recessed portions of encapsulant material 30 over channels or troughs 26 provide alignment guidance for the dicing of the substrate 10 into discrete semiconductor devices 34. Again, channels or troughs 26 extend below the layer 16 of integrated circuitry 18 on active surface 14 of semiconductor substrate 10. As is shown, the substrate 10 has been singulated into discrete semiconductor devices 34. The sloped sidewalls of the encapsulant material 30 extend past the edges of layer 16 exposed by, for example, scribing with a wafer saw in such a manner as to provide a substantially hermetic seal against water, dust, and other contaminants that might otherwise damage or otherwise compromise the integrity and operation of semiconductor device 34. The intermediate conductive elements 20, if not completely covered but only partially covered but supported at their peripheries by encapsulant material 30 as shown in broken line at 36, may in fact be used for connection to higher-level packaging without further disposition of external conductive elements 32 thereon and also without planarization, except to an extent necessary to ensure good exposure of the conductive materials of intermediate conductive elements 20. If completely covered, the upper ends of intermediate conductive elements 20 may be exposed by abrasive planarization, or the encapsulant material 30 selectively etched to expose the upper ends.